# Rx2 Device comparison table

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This table helps you to decide which Philips Rx2 devices best fits your application. The device comparison below lists the various features along with their descriptions.

| Feature | P89C51Rx2Hxx | P89C51Rx2xx/01 | P89LV51RD2 and P89V51RD2 | Comments |
|---|---|---|---|---|
| **Part Number** | P89C51Rx2Hxx(x) 5 V | P89C51Rx2xx(x) 5 V | P89V51RD2 (5 V)<br>P89LV51RD2 (3 V) | Part number and addition of 3 V device |
| **Parallel Programming Algorithm** | When using a parallel programmer, be sure to select P89C51Rx2Hxx(x) devices | When using a parallel programmer, be sure to select P89C51Rx2xx(x) device (no more letter 'H') | Select P89V51RD2 or P89LVRD2 respectively. Bootloader needs to be reprogrammed when security bit is set | Parallel programming algorithm Bootloader for V and LV devices can be obtained from the internet (www.semiconductors.philips.com/microcontrollers) |
| **Signature Bytes** | P89C51RD2 = 15h C2h 80h<br>P89C51RC2 = 15h C2h 89h<br>P89C51RB2 = 15h C2h 8Bh | P89C51RD2 = 15h C2h 82h<br>P89C51RC2 = 15h C2h 8Ah<br>P89C51RB2 = 15h C2h 8Ch<br>P89C51RA2 = 15h C2h 8Fh | P89V51RD2 = BFh 91h<br>P89LV51RD2 = BFh 90h | New Signature Bytes; (for parallel programmer identification) |
| **Clock Mode Selection Using Parallel Programmer** | 6-clk default, OTP configuration bit to program to 12-clk mode using parallel programmer (cannot be programmed back to 6-clk) | 12-clk default, Flash configuration bit to program to 6-clk mode using parallel programmer (can be re-programmed back to 12-clk) | 12-clk default, Flash configuration bit to program to 6-clk mode using parallel programmer (can be re-programmed back to 12-clk) | More flexibility for the end user, more compatibility to older P89C51Rx+ parts |
| **Clock Mode Selection Using ISP/IAP** | N/A | 6-clock/12-clock mode programmable via ISP/IAP | 6-clock/12-clock mode programmable via ISP/IAP | Clock mode can now be selected via ISP or IAP |
| **Clock Mode Selection Via Software** | N/A | 6-clock/12-clock mode programmable "on the fly" by SFR bit X2 (CKCON.0) | 6-clock/12-clock mode programmable "on the fly" by SFR bit X2 (FST.3) | Clock mode can now be changed by software |
| **Peripheral Clock Modes** | N/A | Peripherals can run in 12-clk mode while CPU runs in 6-clk mode (software control) | N/A | |
| **Flash Block Structure** | 2 8-Kbyte blocks, 1 to 3 16-Kbyte blocks | 2 to 16 4-Kbyte blocks | 512 blocks of 128bytes | More flexibility, shorter block erase times |
| **ISP** | 2 modes of entry –<br>1. Status Byte not equal 0<br>2. PSEN = Low, P2.7 and P2.6 = High after Reset | 2 modes of entry –<br>1. Status Byte not equal 0<br>2. PSEN = Low after Reset | On power-up reset, UART will attempt to auto baud. User code will be executed after 400 ms of auto baud failure | Simplified ISP entry |
| **New Features** | N/A | N/A | SPI<br>On-Chip Debugger (SoftICE)<br>Serial Number for serialization | Added Serial peripheral and more software features |

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